Remarks

Applicant thanks the Examiner in advance for a careful examination and allowance of this application.

The specification amendments conform to those made in the earlier applications.

New claims 25-51 better define the claimed inventions.

The enclosed Petition to Make Special explains the grounds for the petition in accordance with the rules.

The enclosed Information Disclosure Statement A briefly discusses the art cited on the electronically filed IDS-A and the enclosed PTO-1449 forms.

Support for claim limitations

Some claim limitations find support in the present application through incorporation by reference of portions of US 5,001,713. That patent issued from Application No. 07/308,272, filed February 8, 1989. The present application as filed included this incorporation by reference. See the original application, page 11, end of the first paragraph.

The present application provides a disclosure of the Event Qualification Module, EQM, 32 in Figure 7. The present application concludes the description of the structure depicted in Figure 7 by saying: "The operation and protocol of the Event Qualification Module are described in" the cited US 5,001,713 and US 5,103,450.

In Figure 6 of US 5,001,713, the drawing depicts start and stop expected data section 98, which supports the "expected data memory" of claims 25, 26, and 27. In the incorporated patent, column 9, line 63, the text says: "The start expected data register 100 and stop expected data register 102 are connected to a multiplexer 114, which outputs the signal EXPDAT." This is the same signal EXPDAT0-15 depicted in Figure 7 of the present application.

The claims

Independent claim 25 defines an integrated circuit having several elements formed on a substrate.

Operating circuits include an operating bus of plural leads for carrying normal operating signals

A serial data input lead and a serial data output lead are coupled together for carrying serial data signals on the substrate.

An expected data memory has plural expected data storage locations for storing serial data signals representing an expected data pattern. The expected data memory has at least one input coupled to the serial data input lead and to the expected data storage locations for receiving the expected data pattern signals from the serial data input lead.

A comparator has first inputs coupled to the operating bus and has second inputs coupled to the expected data memory for

comparing at least some of the normal operating signals to corresponding ones of the expected data pattern signals.

A command register has plural command storage locations for storing serial data signals representing commands. The command register has a control input and has a serial input coupled to the serial data input lead and to the command storage locations for carrying the command signals to the storage locations. The command register has a serial output coupled to the serial data output lead.

A data register has plural data storage locations and data inputs coupled to the data storage locations and to the first inputs of the comparator for carrying the normal operating signals to the data storage locations The data register has a control input and a serial input coupled to the serial data input lead and to the data storage locations for carrying the serial data signals to the data storage locations The data register has a serial output coupled to the serial data output lead and the data storage locations for carrying the signals in the data storage locations to the serial data output lead.

A mode select input lead carries a mode select signal.

A serial data clock input carries a serial data clock signal.

An access port includes control circuitry and has a command control output coupled to the control input of the command register, a data control output coupled to the control input of the data register, a first input coupled to the mode select input lead and a second input coupled to the serial data clock input lead.

The control circuitry is operable selectively to control shifting of the serial data signals between the serial data input lead and the serial data output lead, and into and out of the command register, into and out of the data register, and to the expected data memory responsive to the mode select signal and the serial data clock signal.

Independent claim 26 defines an electrical circuit comprising several elements.

Operating circuits include an operating bus of plural leads for carrying normal operating signals.

A serial data input lead and a serial data output lead.

An expected data memory has plural expected data storage locations for storing signals representing an expected data pattern. The expected data memory has at least one input coupled to the serial data input lead and to the expected data storage locations for receiving the expected data pattern signals from the serial data input lead.

A comparator has first inputs coupled to the operating bus and second inputs coupled to the expected data memory.

A command register has plural command storage locations, a control input, a serial input coupled to the serial data input lead and a serial output coupled to the serial data output lead.

A data register has plural data storage locations, a control input, data inputs coupled to the first inputs of the comparator, a serial input coupled to the serial data input lead and a serial output coupled to the serial data output lead.

A mode select input lead carries a mode select signal.

A serial data clock input lead for carries a serial data clock signal.

An access port includes control circuitry. The access port has a first input coupled to the mode select input lead, a second input coupled to the serial data clock input lead, at least one command register control output coupled to the command register control input, and at least one data register control output coupled to the data register control input.

The operating circuits, the expected data memory, the comparator, the serial data input lead, the serial data output lead, the command register, the data register, the mode select input lead, the serial data clock input lead, and the access port are permanently integrated together.

Independent claim 27 defines an electrical circuit comprising several elements.

Operating circuits include an operating bus of plural leads for carrying normal operating signals.

A serial data input lead and a serial data output lead.

An expected data memory has plural expected data storage locations for storing signals representing an expected data pattern. The expected data memory has at least one input coupled to the serial data input lead and to the expected data storage locations for receiving the expected data pattern signals from the serial data input lead.

A comparator has first inputs coupled to the operating bus and second inputs coupled to the expected data memory.

A data register has plural data storage locations, a control input, data inputs coupled to the first inputs of the comparator, a serial input coupled to the serial data input lead, and a serial output coupled to the serial data output lead.

A mode select input lead carries a mode select signal.

A serial data clock input lead carries a serial data clock signal.

An access port includes control circuitry. The access port has a first input coupled to the mode select input lead, a second input coupled to the serial data clock input lead, and at least one data control output coupled to the control input of the data register.

The operating circuits, the expected data memory, the comparator, the serial data input lead, the serial data output lead, the data register, the mode select input lead, the clock input lead, and the access port are permanently integrated together.

Selected art

Applicant relies upon the combination of all the limitations in the independent claims for patentability and not any general description.

Independent claims 25, 26, and 27 distinguish over the cited art by requiring: operating circuits; an expected data memory coupled to a serial data input lead; a comparator having first inputs coupled to the operating circuits and second inputs coupled to the expected data memory; a data register coupled to the first inputs of the comparator, to the serial data input lead, and to a serial data output lead; a mode select input lead; a serial data clock input lead; and an access port.

These elements are either formed on a substrate or are permanently integrated together.

Claims 25 and 26 further require a command register.

The following cited art fails to disclose an expected data memory coupled to a serial data input lead, and a data register coupled to the first inputs of a comparator and the serial data input and output leads, in the defined combinations.

Applicant could repeat a statement of these distinguishing limitations after the discussion of each following cited patent to meet the requirements of 37 CFR 1.111(b) and (c). Since each cited patent and the cited patents in combination fail to teach or suggest these distinguishing limitations, applicant will rely upon

the preceding statement of the distinguishing limitations, without repetition.

US Patents

US 4,023,142 to Woessner discloses a common reliability and service bus connected to each functional unit of LSI apparatus. The bus provides for an addressed unit to go through an operation after a test pattern has been loaded into the unit while the system continues to operate concurrently. Figure 4 depicts a control system adapter 200 with shift register configuration 210. Data bits 0-7 appear to be loaded in parallel into Diagnostic Address Register 175, Mode Register 1 120, Mode Register 2 180, Mode Register 3 185, and Shift Register 170. Level Shifting Serial Design latches 210 form a scan path. An exclusive OR circuit 400 compares the data from shift register 210 to be compared serially, bit-by-bit, with an expected data pattern loaded into register 170.

US 4,108,359 to Proto discloses a device for detecting errors in the execution of a sequence of coded instructions. A feed-back shift register generates a digital sequence combined with the sequence of instructions to compute a unique sequence check word that is compared to a stored, known good check word. This patent was cited in parent patent US 5,905,738.

US 4,268,902 to Berglund, et al. discloses a maintenance interface for interfacing a service processor and a central processor operating synchronously to each other. The interface circuitry synchronizes the service processor to the central processing unit and decodes commands from the service processor.

The interface circuitry also establishes communication from the central processing unit to the service processor and resolves communication contention between the processors.

Circuitry provides independent control of the clocks to each functional unit or shift ring (scan path) and the functional unit interface signals to other functional units or arrays. The interface includes a Level Sensitive Scan Design (LSSD) testing system with four separate shift rings and provides degating of central processing unit interfaces as required for this testing approach.

US 4,312,066 to Bantz, et al. discloses an interface between a host processor and a diagnostic/debugging processor that troubleshoots the hardware and software of the host processor. The host uses the Level Sensitive Scan Design rules.

The disclosed system allows the machine state and memory of the Host CPU to be captured at the end of an instruction or at the end of a cycle. It further allows selective reading and writing of the memory state by conditioning the H-machine with state information that will cause words from or to memory to be transferred to the D-machine. The system allows control over interruption, channel activity and address translation and provides a diagnostic CPU with its own memory to perform diagnostic and debug functions.

US 4,504,784 to Goel, et al. discloses chips in a module or any second level package. The test mechanism built into each chip will be used in place of mechanical probes to perform a chip-in-place test and interchip wiring test of the package. Level

sensitive scan design rules need to be used for each chip and for the package clock distribution network. Divisional patent of US 4,441,075 and corresponds to US 4,494,066. This patent was cited in parent patent US 5,905,738.

US 4,514,845 to Starr discloses locating a bus fault by placing devices in a high impedance state and sensing current flow between devices. This patent was cited in parent patent US 5,905,738.

US 4,628,511 to Stitzlein, et al. discloses recording pre- and post-failure events to analyze signal activity on an input/output channel to determine failing equipment. This patent was cited in parent patents US 5,905,738 and US 6,131,171.

US 4,674,089 to Poret, et al. discloses an in-circuit emulator (ICE). Capture logic 15 captures the contents of the program address register (PAR), the internal data bus (IDB), and various microprocessor 13 control (CONTROL) lines. The capture logic 15 provides outputs on lines 45 to trace circuits 25. Trace circuits 25 use a FIFO buffer to transfer the captured data to the output pins 31 of the chip 11. A content addressable memory 17 and a software programmable logic array 21 operate as a finite state machine to perform testing. The content addressable memory 17 determines the status of the processor and compares it with a set of four possible word recognizers with comparators 61. The content addressable memory 17 and software programmable logic array are apparently loaded from the microprocessor 13 over lines 41 through mode control 27 and lines 43.

US 4,701,920 to Resnick, et al. discloses built-in self test circuitry 10 for LSI circuit chips. The test circuitry includes a serial scan path (TDI-TDO) and control signal logic 42. Input register 36 applies test signals to the main logic function 14 and output register 38 receives output signals from the main logic function 14.

US 4,788,683 to Hester, et al. discloses a converter between a system processor and a support processor for controlling testing of the system processor. A parallel-to-serial and serial-to-parallel converter conveys LSSD test signals between the two processors.

In Fig. 3A, debug logic includes an instruction address comparator 11 and an instruction op-code comparator 12. Select logic 13 determines which comparator output is selected. An instruction compare address register 14 and an op-code compare address register 16 are accessible by the LSSD scan strings on line 30a, and contain the desired instruction and op-code compare values, respectively. In addition to the selection between stop on instruction address or op-code made by the selection logic 13, stop enable logic 17 contains a single latch bit to enable the stop-on-address function.

One output 18 is provided for the compare output and a separate output 19 is provided for the stop-on-address function. The compare output from 18 can be used as a sync pulse to an external logic analyzer. The stop output from 19 is used in conjunction with the external clock generator to disable the clocks when the stop address is detected. A third output 21 is provided which toggles each time an instruction is executed. This

"Instruction Complete" output is required to implement an instruction single step function, since instructions may take more than one cycle to execute.

US 4,817,093 to Jacobs, et al. discloses testing a multi-chip packaged structure by isolating the one chip under test, applying test signals to that chip, creating a signature of the response signals from that chip and comparing the signature to that of a known good chip. This patent was cited in parent patent US 5,905,738.

US 4,887,267 to Kanuma discloses a logic circuit having a FIFO memory circuit to store values from a test node. The FIFO memory then is unloaded to trace the outputs of such as the states of an internal bus. This patent was cited in parent patent US 5,905,738.

US 4,926,425 to Hedtke, et al. discloses a system for testing successive component groups separated by accessible nodes. The process observes data at the nodes and supplies test data to the nodes. This patent was cited in parent patent US 5,905,738.

US 4,947,357 to Stewart, et al. discloses a circuit board carrying plural integrated circuits, each with an internal scan chain. The scan input of each integrated circuit is connected to a system scan controller 26. The scan outputs of the integrated circuits are connected to multiplexer 30 for selective testing of individual integrated circuits.

US 5,084,874 to Whetsel discloses a testing buffer register 12. See Figure 2. The test cell can also include compare and

other logic. See Figures 6 and following. Corresponds to US 5,495,487; US 5,602,855; US 5,631,911; US 6,081,916; US 6,304,987; and US 6,611,934. This patent was cited in parent patent US 5,905,738.

This patent is believed to be not prior art to the present application. This patent is to the same inventor as in this application and issued on January 28, 1992, after the filing date of June 30, 1989 of the present application.

Other Documents

The Intel 80386 Programmer's Manual discloses the debugging features of the 80386 architecture and the registers used for debugging. The principal debugging support takes the form of debug registers. The debug registers support both instruction breakpoints and data breakpoints. A reserved debug interrupt vector permits the processor to automatically invoke a debugger task or procedure when an event occurs that is of interest to the debugger. The debug registers are accessed by variants of the MOV instruction.

The Intel Microprocessor and Peripheral Handbook discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

The Intel Microprocessor and Peripheral Handbook, Section 2.11.2 TLB Testing, also discloses that there are two TLB (Translation Lookaside Buffer) testing operations. One is to write entries into the TLB. The other is to perform TLB lookups. C: is the command bit. A "0" written into this bit causes an immediate write into the TLB entry. A "1" written into this bit causes an immediate TLB lookup.

The Intel386™ DX Microprocessor data sheet discloses the debugging features of the 80386 architecture and the registers used for debugging. On the page of the data sheet following the page carrying Fig. 2-13, Debug Registers, and at the paragraph bridging the left and right columns, the data sheet explains that the Debug registers can only be accessed in Real Mode. At Section 3.1, REAL MODE INTRODUCTION, Real Mode operation allows access to the 32-bit register set of the 80386.

In Section 2.11.2 TLB Testing, when testing, the Translation Lookaside Buffer must be turned off (PG=0 in CRO) to enable the TLB testing hardware and avoid interference with the test data being written to the TLB. There are two TLB testing operations: 1) write entries into the TLB, and 2) perform TLB lookups. Two Test Registers, shown in Figure 2-12, are provided for the purpose of testing. TR6 is the "test command register", and TR7 is the "test data register". Figure 2-12 depicts the fields within the registers.

C: is the command bit. For a write into TR6 to cause an immediate write into the TLB entry, write a 0 into this bit. For a write into TR6 to cause an immediate TLB lookup, write a 1 to this bit.

The Joint Test Action Group paper, January, 1988, discloses an early version of the standard for a boundary scan test architecture.

The Kuban paper discloses a built-in self-test of a Motorola microprocessor having a serial architecture. The self-test is based on a ROM-driven signature analysis technique. The resulting signature is output from the microprocessor for external examination of the signature.

Referring to Figure 9 and the description on page 39, right-hand column, the operating mode of the MC6804P2 is controlled by RESET, MDS, PA7, and PA6. When RESET is brought high, the levels on the MDS, PA7, and PA6 pins are sampled, and the appropriate mode is selected. The two test modes are invoked by a high on the MDS and PA7 pins. The functional test is then entered if the PA6 pin is low; otherwise, a high on PA6 invokes the ROM verify test. The self-test fixture provides a good/bad indicator for the ROM verify test.

The Whetsel (January, 1988) paper discloses an overview of the JTAG IC test architecture. The disclosed architecture is readily expandable to accommodate boundary scan and other IC test structures such as built-in self test (BIST) and internal core scan design. Figure 8 depicts a boundary register bit.

Conclusion

Claims 25 through 51 are allowable.

The specification is in allowable form and the claims distinguish over the art. Applicant requests reconsideration or further examination of this application.

Respectfully submitted,

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